FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
09669/005001	
U S APPLICATION NO (IF KNOWN, SEE 37 CFR	
09/890226	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/00098	18 January 2000	27 January 1999

TITLE OF INVENTION

INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING SAID DEVICE

APPLICANT(S) FOR DO/EO/US

Yves REIGNOUX and Eric DANIEL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☒ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Amendments made at the time of filing the international application (pages 2, 3, 3bis, 8, and 9)
French Search Report dated 10/14/1999

APPLICATION NO.	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/890226	PCT/FR00/00098	09669/005001

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO **$970.00**	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO **$840.00**	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$690.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$670.00**	
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$96.00**	

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$840.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	10 - 20 =	0	x $18.00	**$0.00**	
Independent claims	3 - 3 =	0	x $78.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
	TOTAL OF ABOVE CALCULATIONS =			**$840.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**. ☐				**$0.00**	
	SUBTOTAL =			**$840.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
	TOTAL NATIONAL FEE =			**$840.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
	TOTAL FEES ENCLOSED =			**$840.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$840.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **500-591** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Jonathan P. Osha
ROSENTHAL & OSHA, L.L.P.
700 Louisiana, Suite 4500
Houston, Texas 77002
United States of America

Telephone: 713/228-8600
Facsimile: 713/228-8778

SIGNATURE

Jonathan P. Osha
NAME

33,986
REGISTRATION NUMBER

July 27, 2001
DATE

ATTORNEY DOCKET NO. 09669/005001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yves REIGNOUX et al. Art Unit:
Serial No.: Examiner:
Filed: July 27, 2001
Title: INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING SAID DEVICE

Assistant Commissioner for Patent
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination, please amend the application as follows:

IN THE SPECIFICATION

Page 1, between line 5 and line 6, insert: -- FIELD OF THE INVENTION--;

Page 1 between line 15 and line 16, insert: --BACKGROUND OF THE INVENTION--;

Page 2, between line 27 and line 28, insert: --SUMMARY OF THE INVENTION--;

Page 4, between line 6 and line 7, insert: --BRIEF DESCRIPTION OF THE DRAWINGS--; and

Page 4, between line 16 and line 19, insert: --DETAILED DESCRIPTION--.

REMARKS

Full examination and favorable action are requested.

Please charge any fees, or make any credits, to Deposit Account No. 500-591, Reference No. 09669/004001.

Date: 7/27/01

Jonathan P. Osha
Reg. No. 33,986

Rosenthal & Osha L.L.P.
700 Louisiana Street, Suite 4550
Houston, TX 77002

Telephone: 713/228-8600
Facsimile: 713/228-8778

17966_1.DOC

INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING SAID DEVICE

The present invention relates to an integrated circuit device, an electronic unit for smart cards using the integrated circuit device and a method for manufacturing said device.

More specifically, the present invention relates to the manufacturing of a semiconductor chip in which integrated circuits are formed, having a structure such that electronic units for smart cards of reduced thickness can be manufactured.

It is known that smart cards used in particular as banking cards, such as an identification card, or also as a payment card for different services, are essentially made of a plastic material body of rectangular parallelepiped shape in which is inserted an electronic unit most often made of a semiconductor chip attached to an insulating substrate provided with external electrical contact pads. These external pads enable electrical connection between the circuits in the semiconductor chip and circuits in a read-write device when the card is inserted within such a device.

According to the prevailing standards, the card body should have a thickness of about 0.8 mm. It should be understood that the thickness of the electronic unit is therefore one of its critical parameters, and facilitates the insertion of the electronic unit within the card body and ensures a proper mechanical coupling between the card body and the electronic unit as well as the mechanical integrity of the electronic unit.

In the appended Figure 1, a vertical cross section of an electronic unit for smart cards made according to a known technique is shown. Electronic unit 10 is essentially comprised of a semiconductor chip 12 in

which integrated circuits are formed, this chip having an active face 14 provided with electrical connection terminals 16. The semiconductor chip 12 is attached to an insulating substrate 18 through an adhesive layer 19. The external face 18a of the insulating substrate is provided with external contact pads 20 to be contacted with the electrical contacts of the read-write device. Terminals 16 of chip 12 are connected to external pads 20 through leads such as 24. According to a known method, the

insulating substrate comprises windows 26 with electrical leads 24, so that the use of a doubled-faced printed circuit is avoided. In order to ensure electrical integrity of chip 12 and electrical leads 24, they are encapsulated with an insulating material 26 such as an epoxy resin.

In some cases, the wire leads can be replaced with other electrically conducting elements for connecting the chip terminals to external pads on the insulating substrate.

With such a manufacturing technology, an electronic unit having an overall thickness of about 0.6 mm, is obtained, to be compared with the 0.8 mm thickness of the card body.

Techniques that would allow reducing this thickness are difficult to implement. They could consist in reducing the chip thickness, which is conventionally of the order of 180 μm, but this would unacceptably reduce chip strength. One could also reduce the thickness caused by the curvature of electrical wires 24 or similar electrical connection elements. This, however, requires using the so-called "Wedge bonding" technology which is of costly implementation. Finally, it could be contemplated to reduce the thickness of the insulating resin of encapsulation 26. Such a reduction would however reduce the strength of the electronic unit as a whole.

US 5,155,068 discloses a method of manufacturing an electronic unit for smart cards. According to this method a semiconductor chip comprises an active face provided with metallic wire layers. Connections are formed between these metallic wire layers and a substrate provided with electrical contacts. An acryl or epoxy resin is then applied for attaching the semiconductor chip to the substrate with its electrical contacts. The method is of costly implementation.

A first objet of the present invention is to provide an integrated circuit device permitting the

manufacturing of an electronic unit for smart cards having a reduced thickness while not having the drawbacks of the above-mentioned techniques.

To achieve this object, according to the invention, the integrated circuit device is characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 μm, and

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to said side surface.

An electronic unit for smart cards can be realized from such an integrated circuit device. The electronic unit further comprises an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the inner face of the substrate, and a plurality of electrical leads, each lead having a first end connected to a contact terminal and a second end connected to an external contact pad and lying entirely between the plane containing the second face of the complementary chip and the insulating substrate.

It should be understood that, due to the reduced thickness of the active layer, on the active face of which contact terminals are formed, these contact terminals are close to that face of the integrated circuit device which is attached to the insulating substrate when the electronic unit is formed. It should also be understood that, due to the presence of recesses which open into the side surface of the complementary layer, it is possible, when forming the electronic unit, to provide connection in the electric wires which are

integrally provided below the plane that includes the upper face of the complementary layer. It should be understood that the resulting thickness of the electronic unit is substantially reduced relative to the thickness of an electronic unit of the previously described type.

The present invention also relates to a method for manufacturing an integrated circuit device from:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, and

- a complementary chip having a first face, a second face and a side face, the complementary chip including a plurality of recesses, each recess extending through the whole thickness of the complementary chip, wherein the method is characterized in that it comprises the following steps:

- an attachment step wherein the first face of the complementary chip is attached to the active face of the active chip so that a recess of the complementary chip extends from above a contact terminal of the active chip to the side surface of the complementary chip; and

- an etching step wherein the active chip is etched from its second face so as to provide it with a thickness of less than 100 µm.

It should be understood that according to this method, the starting element is an active layer having a standard thickness, namely about of 180 µm, which active layer is attached to the complementary layer, which itself has a certain thickness. Thus, an assembly is obtained with a sufficient thickness for etching the non-active face of the active layer while complying with overall dimensions such that the assembly maintains a sufficient mechanical strength.

Other features and advantages of the present invention will be apparent from the following detailed description of an embodiment of the invention given by way of non limiting example in reference to the accompanying drawings, in which:

Figure 1, already described, shows a vertical cross-section of an electronic unit for a standard smart card.

Figures 2a and 2b show a vertical cross-section of two manufacturing steps of the electronic unit according to this invention;

Figure 3 shows a horizontal cross-section of the electronic unit along line III-III of Figure 2b; and

Figures 4a to 4c show the various steps of the method for manufacturing the integrated circuit device.

Referring first to Figures 2 and 3, a description will be given of the integrated circuit device or electronic chip and the electronic unit using the same.

The integrated circuit device 30 is essentially comprised of an active layer 32 of a semiconductor material, typically silicon, into which the different integrated circuits are formed. This active layer 32 has an active face 34 into which electric contact terminals and an attachment face 38 are formed. The integrated circuit 30 also comprises a complementary layer 40 whose first face 42 is attached through any appropriate means, for example, an intermediate sealant layer formed of a polyimide, to the active face of active layer 32 and whose upper face 44 is free. Complementary layer 40 may also be advantageously made of silicon, but other materials having physical characteristics similar to silicon, in particular in what concerns it thermal expansion coefficient, could be used. One of the functions performed by complementary layer 40 is to form a protective layer against fraud attempts that could be performed with respect to the active layer integrated circuits.

As more clearly shown in Figure 3, complementary layer 40 is provided with recesses such as the one shown in 46 (in the given example, there are five connection terminals 36 and five recesses 46). Each recess 46 extends over the whole thickness of the complementary layer and extends from contact terminal 36 to the side surface 48 of complementary layer 40. In other words, these recesses open laterally into the complementary layer.

According to the above described embodiment, the thickness e_1 of the complementary layer is 140 µm and the thickness e_2 of the active layer is 40 µm. Thus, the total thickness of the integrated circuit device is 180 µm, which corresponds to the thickness of a standard semiconductor chip.

More generally, the thickness of the active layer is less than 100 µm, which reduced thickness can be obtained by resorting to the manufacturing method described below. Still preferably, thickness e_2 of the active layer ranges from 5 to about 50 µm.

The thickness of the active layer is thus significantly greater than that of the semiconductor chip. In particular, this leads to a thinner unit, since the lead wires are effectively located, according to a preferred embodiment of the present invention, within the overall thickness of the assembly formed by the complementary layer and the semiconductor chip that constitutes the active layer.

The complementary layer covers substantially entirely or entirely the active face of the active layer except, of course, for the recesses. More specifically, the surface area of the active face of the active layer is substantially the same as the surface area of the first face of the complementary layer after subtracting the surface area corresponding to the recesses formed in said complementary layer. Therefore, it is possible to process the active layer so as to reduce its thickness down to the desired value. In addition, the active

layer/complementary layer assembly is more resistant to the mechanical strains it may undergo, since the complementary layer protects the active layer.

Moreover, it should be noted that there are advantageously as many recesses as connection terminals in the semiconductor chip and that such recesses represent a reduced portion of the total surface area of the complementary layer.

For forming the electronic unit, the integrated circuit device 30 is attached to an insulating support 50 by means of a layer of adhesive material 52, the external face 54 of the insulating substrate being provided with external electrical contact pads 56. Windows such as window 58 are provided within the insulating substrate in front of each of pads 56. A lead wire 60, for example, made of gold, is attached, on the one hand, to the connection terminal 36 and, on the other hand, to the back face of an external electrical contact pad 56 through window 58. It should be understood that because of the very small thickness of active layer 32, terminals 36 are close to the insulating substrate 50. This allows for the whole bent lead wire 60 to be located below plane PP', which includes the upper face 44 of complementary layer 40.

The same would hold if the lead wires were replaced by elongated electrical connection elements.

In order to complete the electronic unit, the encapsulation 62 only needs to be formed, with its total thickness h reduced thanks to the above described provisions.

In the described implementation, the overall thickness h of the encapsulation is 310 μm if thickness of the adhesive layer between the substrate and the integrated circuit device is taken into account. The thickness e_3 of the insulating substrate being typically of 170 μm, the obtained electronic unit has a thickness of 480 μm. This represents a very large thickness reduction relative to standard electronic units.

Referring now to figures 4A, 4B and 4c, the main steps in the manufacture of integrated circuit device 30 will be explained.

In a first step shown in Figure 4A, a silicon wafer is diced by means of any appropriate method allowing the complementary layer 40 to be formed with its recesses 46. This layer could be made of any other material. Its thickness e_1 preferably ranges from 100 to 200 µm.

Then, in a step shown in Figure 4B, the complementary layer 40 is attached to the active face 72 of a semiconductor chip 50 provided with connection terminals 36. This chip has a standard thickness d of about 180 µm.

Finally, in a step shown in Figure 4C, the non-active face 74 of chip 70 is processed by any appropriate method so as to reduce its thickness e_2 to a typical value of 40 µm, and active layer 32 is obtained.

Due to the presence of complementary layer 40, the integrated circuit device 30 has an overall thickness of about 180 µm in the considered example. One thus obtains a component of sufficient mechanical strength although the active layer 32 by itself has a thickness e_2 which does not provide such mechanical strength properties. Therefore, as already explained, the main advantage of the thus obtained component is that the contact terminals 36 are in very close proximity to the component attachment face 38.

CLAIMS

1. An integrated circuit device, characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 µm, and

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to said side surface, the complementary chip having a larger thickness than the active chip.

2. An integrated circuit device according to claim 1, characterized in that the thickness of the active layer ranges from 5 to 50 µm.

3. An integrated circuit device according to claim 2, characterized in that the thickness of the complementary layer ranges from 100 to 200 µm.

4. An integrated circuit device according to any of claims 1 to 3, characterized in that the complementary chip is formed with the same semiconductor material as the active chip.

5. An electronic unit for smart cards, characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 µm,

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip

and extending from above a contact terminal to said side surface, the complementary chip having a larger thickness than the active chip,

- an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the substrate inner face, and

- a plurality of electrical leads, each lead having a first end connected to a contact terminal and a second end connected to an outer contact pad and lying entirely between the plane containing the second face of the complementary chip and the insulating substrate.

6. An electronic unit according to claim 5, characterized in that the insulating substrate includes windows, each window being disposed above an outer electric contact pad.

7. A smart card comprising an electronic unit according to claim 5.

8. A method for manufacturing an integrated circuit device from:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, and

- a complementary chip having a first face, a second face and a side face, the complementary chip including a plurality of recesses, each recess extending through the whole thickness of the complementary chip,

wherein the method is characterized in that it comprises the following steps:

- an attachment step wherein the first face of the complementary chip is attached to the active face of the active chip so that a recess of the complementary chip extends from above a contact terminal of the active chip to the side surface of the complementary chip; and

- an etching step wherein the active chip is etched from its second face so as to provide it with a thickness of less than 100 μm.

ABSTRACT

Integrated circuit device, electronic unit for smart cards using said device and method of manufacturing said device

This invention relates to an integrated circuit device, in particular for manufacturing smart card electronic units for smart cards. It comprises:

an active layer (32) including a semiconductor material within which integrated circuits are formed and having a face (34) provided with a plurality of electrical connection terminals (36) and a second face, wherein said face has a thickness smaller than 100 μm, and

a complementary layer (40) having a first face (42) attached to the active face of the active layer, a second face (44) and a side surface (48), wherein said complementary layer includes a plurality of recesses (46), each recess extending through the whole thickness of the complementary layer, and extending from a contact terminal (36) to said side surface (48).

Figure 2A

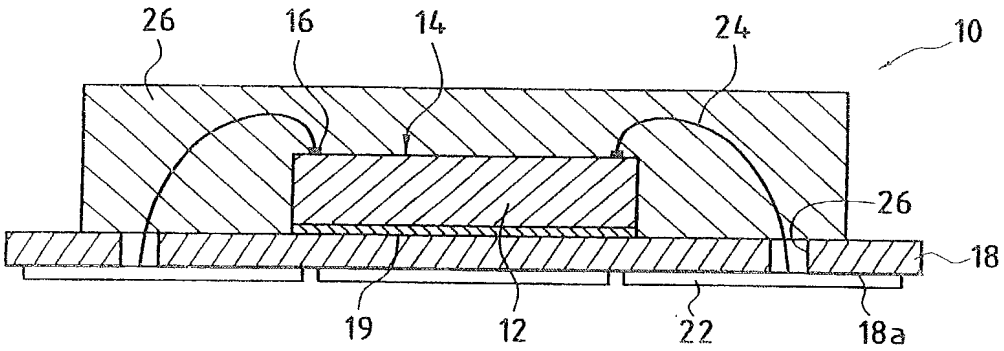

FIG.1
ART ANTERIEUR

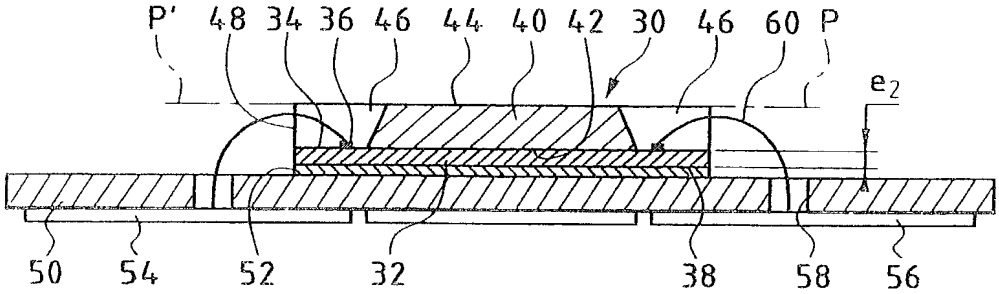

FIG.2A

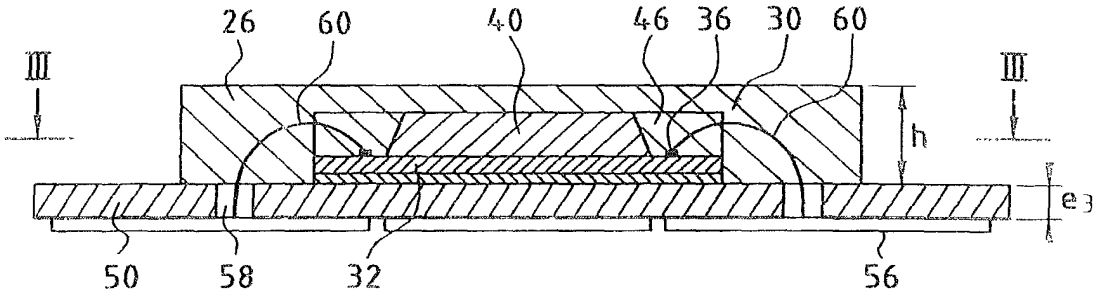

FIG.2B

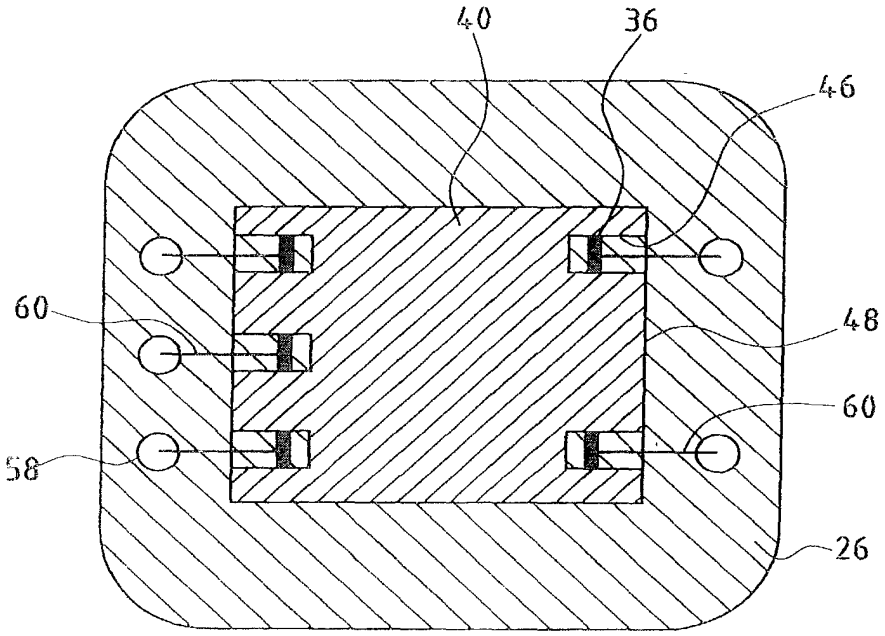

FIG.3

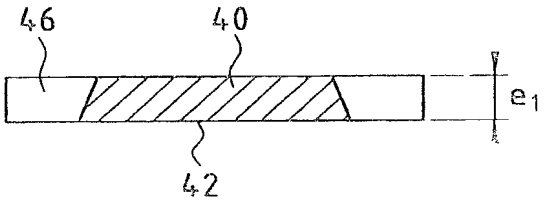

FIG.4A

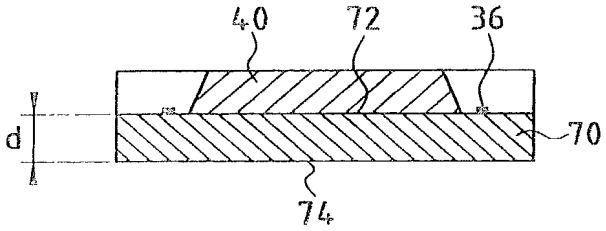

FIG.4B

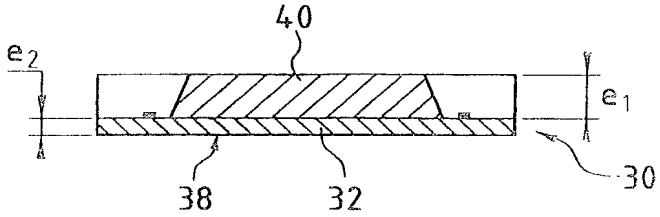

FIG.4C

INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING SAID DEVICE

The present invention relates to an integrated circuit device, an electronic unit for smart cards using the integrated circuit device and a method for manufacturing said device.

More specifically, the present invention relates to the manufacturing of a semiconductor chip in which integrated circuits are formed, having a structure such that electronic units for smart cards of reduced thickness can be manufactured.

It is known that smart cards used in particular as banking cards, such as an identification card, or also as a payment card for different services, are essentially made of a plastic material body of rectangular parallelepiped shape in which is inserted an electronic unit most often made of a semiconductor chip attached to an insulating substrate provided with external electrical contact pads. These external pads enable electrical connection between the circuits in the semiconductor chip and circuits in a read-write device when the card is inserted within such a device.

According to the prevailing standards, the card body should have a thickness of about 0.8 mm. It should be understood that the thickness of the electronic unit is therefore one of its critical parameters, and facilitates the insertion of the electronic unit within the card body and ensures a proper mechanical coupling between the card body and the electronic unit as well as the mechanical integrity of the electronic unit.

In the appended Figure 1, a vertical cross section of an electronic unit for smart cards made according to a known technique is shown. Electronic unit 10 is essentially comprised of a semiconductor chip 12 in

which integrated circuits are formed, this chip having an active face 14 provided with electrical connection terminals 16. The semiconductor chip 12 is attached to an insulating substrate 18 through an adhesive layer 19. The external face 18a of the insulating substrate is provided with external contact pads 20 to be contacted with the electrical contacts of the read-write device. Terminals 16 of chip 12 are connected to external pads 20 through leads such as 24. According to a known method, the

insulating substrate comprises windows 26 with electrical leads 24, so that the use of a doubled-faced printed circuit is avoided. In order to ensure electrical integrity of chip 12 and electrical leads 24, they are encapsulated with an insulating material 26 such as an epoxy resin.

In some cases, the wire leads can be replaced with other electrically conducting elements for connecting the chip terminals to external pads on the insulating substrate.

With such a manufacturing technology, an electronic unit having an overall thickness of about 0.6 mm, is obtained, to be compared with the 0.8 mm thickness of the card body.

Techniques that would allow reducing this thickness are difficult to implement. They could consist in reducing the chip thickness, which is conventionally of the order of 180 μm, but this would unacceptably reduce chip strength. One could also reduce the thickness caused by the curvature of electrical wires 24 or similar electrical connection elements. This, however, requires using the so-called "Wedge bonding" technology which is of costly implementation. Finally, it could be contemplated to reduce the thickness of the insulating resin of encapsulation 26. Such a reduction would however reduce the strength of the electronic unit as a whole.

US 5,155,068 discloses a method of manufacturing an electronic unit for smart cards. According to this method a semiconductor chip comprises an active face provided with metallic wire layers. Connections are formed between these metallic wire layers and a substrate provided with electrical contacts. An acryl or epoxy resin is then applied for attaching the semiconductor chip to the substrate with its electrical contacts. The method is of costly implementation.

A first objet of the present invention is to provide an integrated circuit device permitting the

manufacturing of an electronic unit for smart cards having a reduced thickness while not having the drawbacks of the above-mentioned techniques.

To achieve this object, according to the invention, the integrated circuit device is characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 µm, and
- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to said side surface.

An electronic unit for smart cards can be realized from such an integrated circuit device. The electronic unit further comprises an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the inner face of the substrate, and a plurality of electrical leads, each lead having a first end connected to a contact terminal and a second end connected to an external contact pad and lying entirely between the plane containing the second face of the complementary chip and the insulating substrate.

It should be understood that, due to the reduced thickness of the active layer, on the active face of which contact terminals are formed, these contact terminals are close to that face of the integrated circuit device which is attached to the insulating substrate when the electronic unit is formed. It should also be understood that, due to the presence of recesses which open into the side surface of the complementary layer, it is possible, when forming the electronic unit, to provide connection in the electric wires which are

integrally provided below the plane that includes the upper face of the complementary layer. It should be understood that the resulting thickness of the electronic unit is substantially reduced relative to the thickness of an electronic unit of the previously described type.

The present invention also relates to a method for manufacturing an integrated circuit device from:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, and

- a complementary chip having a first face, a second face and a side face, the complementary chip including a plurality of recesses, each recess extending through the whole thickness of the complementary chip, wherein the method is characterized in that it comprises the following steps:

- an attachment step wherein the first face of the complementary chip is attached to the active face of the active chip so that a recess of the complementary chip extends from above a contact terminal of the active chip to the side surface of the complementary chip; and

- an etching step wherein the active chip is etched from its second face so as to provide it with a thickness of less than 100 μm.

It should be understood that according to this method, the starting element is an active layer having a standard thickness, namely about of 180 μm, which active layer is attached to the complementary layer, which itself has a certain thickness. Thus, an assembly is obtained with a sufficient thickness for etching the non-active face of the active layer while complying with overall dimensions such that the assembly maintains a sufficient mechanical strength.

Other features and advantages of the present invention will be apparent from the following detailed description of an embodiment of the invention given by way of non limiting example in reference to the accompanying drawings, in which:

Figure 1, already described, shows a vertical cross-section of an electronic unit for a standard smart card.

Figures 2a and 2b show a vertical cross-section of two manufacturing steps of the electronic unit according to this invention;

Figure 3 shows a horizontal cross-section of the electronic unit along line III-III of Figure 2b; and

Figures 4a to 4c show the various steps of the method for manufacturing the integrated circuit device.

Referring first to Figures 2 and 3, a description will be given of the integrated circuit device or electronic chip and the electronic unit using the same.

The integrated circuit device 30 is essentially comprised of an active layer 32 of a semiconductor material, typically silicon, into which the different integrated circuits are formed. This active layer 32 has an active face 34 into which electric contact terminals and an attachment face 38 are formed. The integrated circuit 30 also comprises a complementary layer 40 whose first face 42 is attached through any appropriate means, for example, an intermediate sealant layer formed of a polyimide, to the active face of active layer 32 and whose upper face 44 is free. Complementary layer 40 may also be advantageously made of silicon, but other materials having physical characteristics similar to silicon, in particular in what concerns it thermal expansion coefficient, could be used. One of the functions performed by complementary layer 40 is to form a protective layer against fraud attempts that could be performed with respect to the active layer integrated circuits.

As more clearly shown in Figure 3, complementary layer 40 is provided with recesses such as the one shown in 46 (in the given example, there are five connection terminals 36 and five recesses 46). Each recess 46 extends over the whole thickness of the complementary layer and extends from contact terminal 36 to the side surface 48 of complementary layer 40. In other words, these recesses open laterally into the complementary layer.

According to the above described embodiment, the thickness e_1 of the complementary layer is 140 µm and the thickness e_2 of the active layer is 40 µm. Thus, the total thickness of the integrated circuit device is 180 µm, which corresponds to the thickness of a standard semiconductor chip.

More generally, the thickness of the active layer is less than 100 µm, which reduced thickness can be obtained by resorting to the manufacturing method described below. Still preferably, thickness e_2 of the active layer ranges from 5 to about 50 µm.

The thickness of the active layer is thus significantly greater than that of the semiconductor chip. In particular, this leads to a thinner unit, since the lead wires are effectively located, according to a preferred embodiment of the present invention, within the overall thickness of the assembly formed by the complementary layer and the semiconductor chip that constitutes the active layer.

The complementary layer covers substantially entirely or entirely the active face of the active layer except, of course, for the recesses. More specifically, the surface area of the active face of the active layer is substantially the same as the surface area of the first face of the complementary layer after subtracting the surface area corresponding to the recesses formed in said complementary layer. Therefore, it is possible to process the active layer so as to reduce its thickness down to the desired value. In addition, the active

layer/complementary layer assembly is more resistant to the mechanical strains it may undergo, since the complementary layer protects the active layer.

Moreover, it should be noted that there are advantageously as many recesses as connection terminals in the semiconductor chip and that such recesses represent a reduced portion of the total surface area of the complementary layer.

For forming the electronic unit, the integrated circuit device 30 is attached to an insulating support 50 by means of a layer of adhesive material 52, the external face 54 of the insulating substrate being provided with external electrical contact pads 56. Windows such as window 58 are provided within the insulating substrate in front of each of pads 56. A lead wire 60, for example, made of gold, is attached, on the one hand, to the connection terminal 36 and, on the other hand, to the back face of an external electrical contact pad 56 through window 58. It should be understood that because of the very small thickness of active layer 32, terminals 36 are close to the insulating substrate 50. This allows for the whole bent lead wire 60 to be located below plane PP', which includes the upper face 44 of complementary layer 40.

The same would hold if the lead wires were replaced by elongated electrical connection elements.

In order to complete the electronic unit, the encapsulation 62 only needs to be formed, with its total thickness h reduced thanks to the above described provisions.

In the described implementation, the overall thickness h of the encapsulation is 310 μm if thickness of the adhesive layer between the substrate and the integrated circuit device is taken into account. The thickness e_3 of the insulating substrate being typically of 170 μm, the obtained electronic unit has a thickness of 480 μm. This represents a very large thickness reduction relative to standard electronic units.

Referring now to figures 4A, 4B and 4c, the main steps in the manufacture of integrated circuit device 30 will be explained.

In a first step shown in Figure 4A, a silicon wafer is diced by means of any appropriate method allowing the complementary layer 40 to be formed with its recesses 46. This layer could be made of any other material. Its thickness e_1 preferably ranges from 100 to 200 µm.

Then, in a step shown in Figure 4B, the complementary layer 40 is attached to the active face 72 of a semiconductor chip 50 provided with connection terminals 36. This chip has a standard thickness d of about 180 µm.

Finally, in a step shown in Figure 4C, the non-active face 74 of chip 70 is processed by any appropriate method so as to reduce its thickness e_2 to a typical value of 40 µm, and active layer 32 is obtained.

Due to the presence of complementary layer 40, the integrated circuit device 30 has an overall thickness of about 180 µm in the considered example. One thus obtains a component of sufficient mechanical strength although the active layer 32 by itself has a thickness e_2 which does not provide such mechanical strength properties. Therefore, as already explained, the main advantage of the thus obtained component is that the contact terminals 36 are in very close proximity to the component attachment face 38.

CLAIMS

1. An integrated circuit device, characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 μm, and

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip and extending from above a contact terminal to said side surface, the complementary chip having a larger thickness than the active chip.

2. An integrated circuit device according to claim 1, characterized in that the thickness of the active layer ranges from 5 to 50 μm.

3. An integrated circuit device according to claim 2, characterized in that the thickness of the complementary layer ranges from 100 to 200 μm.

4. An integrated circuit device according to any of claims 1 to 3, characterized in that the complementary chip is formed with the same semiconductor material as the active chip.

5. An electronic unit for smart cards, characterized in that it comprises:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, wherein the chip has a thickness of less than 100 μm,

- a complementary chip having a first face attached to the active face of the active chip, a second face and a side surface, wherein the complementary chip has a plurality of recesses, each recess extending through the whole thickness of the complementary chip

and extending from above a contact terminal to said side surface, the complementary chip having a larger thickness than the active chip,

- an insulating substrate having an outer face provided with outer electrical contact pads and an inner face, the second face of the active chip being attached to the substrate inner face, and

- a plurality of electrical leads, each lead having a first end connected to a contact terminal and a second end connected to an outer contact pad and lying entirely between the plane containing the second face of the complementary chip and the insulating substrate.

6. An electronic unit according to claim 5, characterized in that the insulating substrate includes windows, each window being disposed above an outer electric contact pad.

7. A smart card comprising an electronic unit according to claim 5.

8. A method for manufacturing an integrated circuit device from:

- an active chip of a semiconductor material comprising an electrical circuit, the active chip having an active face provided with a plurality of electrical connection terminals and a second face, and

- a complementary chip having a first face, a second face and a side face, the complementary chip including a plurality of recesses, each recess extending through the whole thickness of the complementary chip,

wherein the method is characterized in that it comprises the following steps:

- an attachment step wherein the first face of the complementary chip is attached to the active face of the active chip so that a recess of the complementary chip extends from above a contact terminal of the active chip to the side surface of the complementary chip; and

- an etching step wherein the active chip is etched from its second face so as to provide it with a thickness of less than 100 μm.

ABSTRACT

Integrated circuit device, electronic unit for smart cards using said device and method of manufacturing said device

This invention relates to an integrated circuit device, in particular for manufacturing smart card electronic units for smart cards. It comprises:

an active layer (32) including a semiconductor material within which integrated circuits are formed and having a face (34) provided with a plurality of electrical connection terminals (36) and a second face, wherein said face has a thickness smaller than 100 μm, and

a complementary layer (40) having a first face (42) attached to the active face of the active layer, a second face (44) and a side surface (48), wherein said complementary layer includes a plurality of recesses (46), each recess extending through the whole thickness of the complementary layer, and extending from a contact terminal (36) to said side surface (48).

Figure 2A

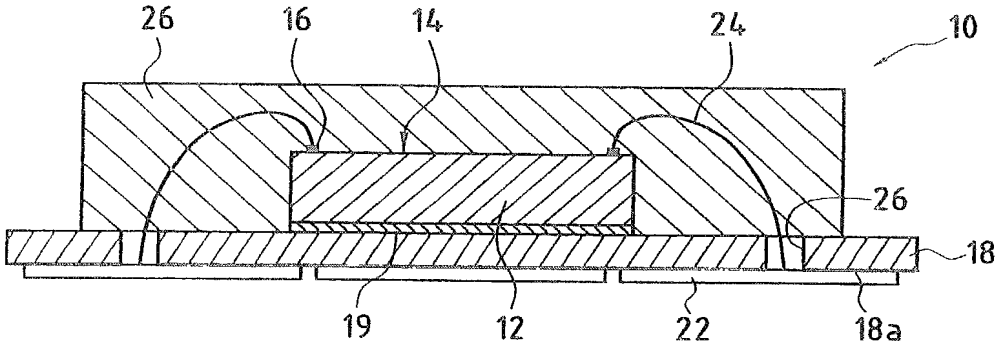

FIG.1
ART ANTERIEUR

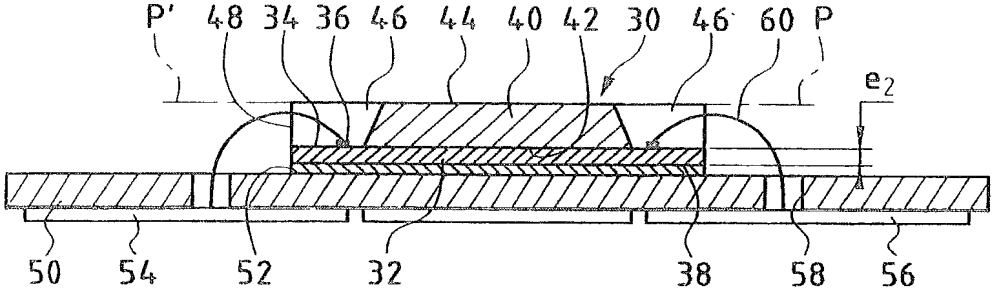

FIG.2A

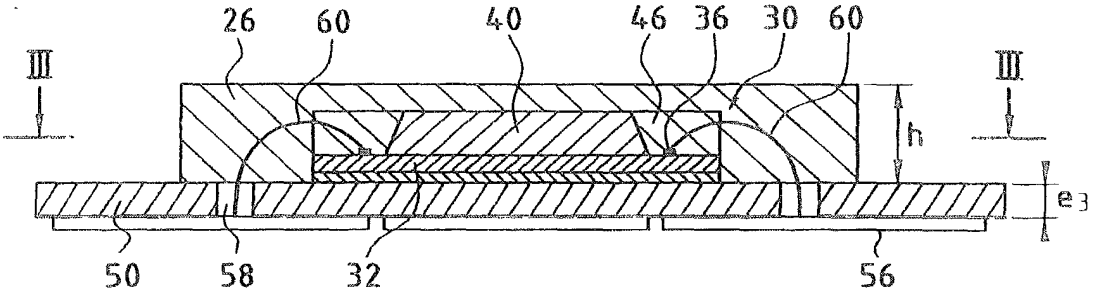

FIG.2B

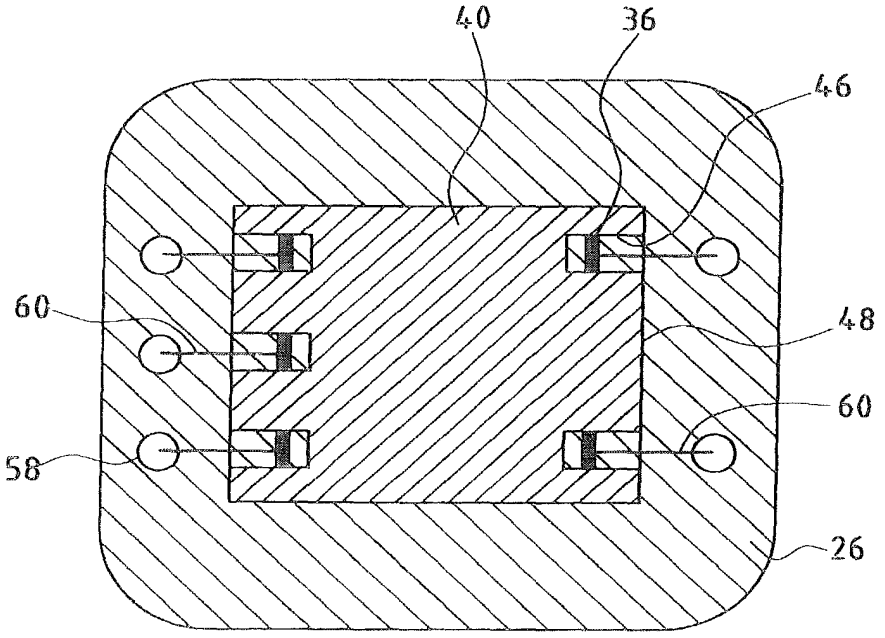

FIG.3

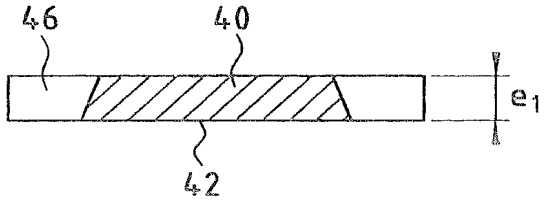

FIG.4A

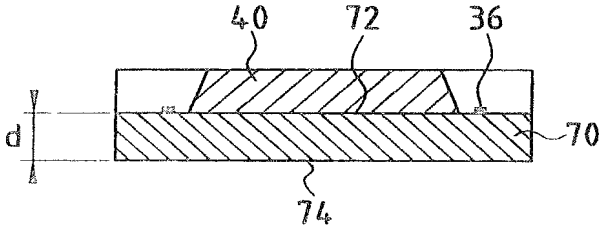

FIG.4B

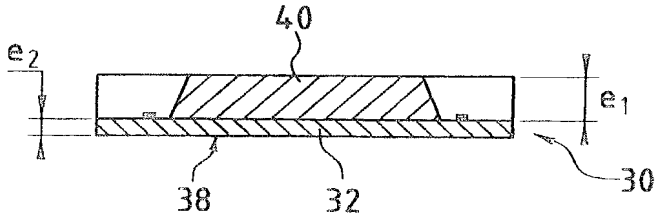

FIG.4C

PTO/SB/01 (03-01)
Approved for use through 10/31/2002 OMB 0651-0032
U.S. Patent and Trademark Office, U S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing **OR** ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	09669/005001
First Named Inventor	Yves REIGNOUX
COMPLETE IF KNOWN	
Application Number	09 /890, 226
Filing Date	July 27, 2001
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATED DEVICE CIRCUIT, ELECTRONIC UNIT FOR SMART CARDS USING SAID DEVICE AND METHOD FOR MANUFACTURING SAID DEVICE.

(Title of the Invention)

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 07/ 27/ 2001 as United States Application Number or PCT International

Application Number 09/ 890, 226 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	Certified Copy Attached? NO
99/ 00858	France	01/ 27/ 1998	☐	☐	☒
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

PTO/SB/01 (03-01)
Approved for use through 10/31/2002 OMB 0651-0032
U S Patent and Trademark Office, U S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

DECLARATION — Utility or Design Patent Application

Direct all correspondence to. ☒ Customer Number or Bar Code Label 22511 OR ☐ Correspondence address below

Name

Address

City | State | ZIP

Country | Telephone | Fax

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR : ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) Yves | Family Name or Surname REIGNOUX

Inventor's Signature | Date 11/05/01

Residence: City La chapelle Saint Mesmin | State | Country France | Citizenship French

Mailing Address 50, Avenue Jean Jaurès – B.P. 620-12

City Montrouge Cedex | State | ZIP 92542 | Country France

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventor

2

Given Name (first and middle [if any]) Eric | Family Name or Surname DANIEL

Inventor's Signature | Date 19/11/01

Residence: City Saint Jean Le Blanc | State | Country France | Citizenship French

Mailing Address 50, Avenue Jean Jaurès – B.P. 620-12

City Montrouge Cedex | State | ZIP 92542 | Country France

☐ Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

Please type a plus sign (+) inside this box → ⊞

PTO/SB/81 (02-01)
Approved for use through 10/31/2002. OMB 0651-0035
U S Patent and Trademark Office, U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it display a valid OMB control number

POWER OF ATTORNEY OR AUTHORIZATION OF AGENT

Application Number	09/890,226
Filing Date	July 27, 2001
First Named Inventor	Yves REIGNOUX
Title	Integrated Device Circuit...
Group Art Unit	
Examiner Name	
Attorney Docket Number	

I hereby appoint:

⊞ Practitioners at Customer Number [ ] → Place Customer Number Bar Code Label here 22511

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please change the correspondence address for the above-identified application to:

☐ The above-mentioned Customer Number.

OR

☐ Practitioners at Customer Number [ ] → *Place Customer Number Bar Code Label here*

OR

☐ Firm *or* Individual Name					
Address					
Address					
City		State		Zip	
Country					
Telephone		Fax			

I am the:

⊞ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

SIGNATURE of Applicant or Assignee of Record

Name	Yves REIGNOUX
Signature	
Date	11/05/01

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

⊞ *Total of 2 forms are submitted.